REMARKS

Applicants respectfully request that claim 1 be amended to include a new limitation. In addition, Applicants respectfully request that new dependent claims 12 and 13 be added. No new matter has been added to the application by virtue of the present amendment. Applicants believe the present amendment does **not** raise new issues requiring further search by the Examiner.

Accordingly, pending claims 1-13 are active in the subject application. It is respectfully requested that the pending claims 1-13 be reconsidered in view of this response.

Claim Rejections – 35 U.S.C. 102 (b)

The Examiner rejected claims 1-8, 10 and 11 under 35 U.S.C. 102(b) as being anticipated by Garbelli et al. (U.S. Patent No. 5,825,628).

Applicants respectfully request that claim 1 be amended to recite the limitation "... a ground plane connected to the ground lead, **the ground plane enclosed within an encapsulating material** ...". Support for Applicants' limitation can be found, for example, in paragraphs [0061], [0062] and by referring to FIGS. 1 and 2 of the present application. Applicants teach a ground plane enclosed within an encapsulating material to provide a ground plane which is electrically isolated from the die and within the chip package so that electric fields are confined to remain within the IC package (FIG. 4, paragraph 0064).

Garbelli et al. neither anticipate nor suggest Applicants' independent claim 1, as amended. Referring to FIG. 3, Garbelli et al. teach device 110 attached on a top surface of substrate 310 and ground plane 342 within substrate 310. Plastic resin 160 (FIG. 1) encapsulates only device 110 and does not encapsulate ground plane 342. Ground plane 342 is surrounded by layers of substrate 310 which consists of different materials (column 4, lines 25-32). Garbelli et al. do not teach or suggest Applicant's limitation of a "... ground plane enclosed within an encapsulating material ...". Applicants invention provides for protection against electric fields radiating from chip packages such as QFP-type or DIP-type chip packages that have a semiconductor device enclosed within an encapsulant. Applicants' invention does not require a multi-layer substrate to provide a ground plane thereby reducing costs associated with chip packaging.

Claims 2-8, 10 and 11 are dependent upon independent claim 1. As discussed above, Garbelli et al. do not teach Applicants' limitation of "... a ground plane connected to the ground lead, **the ground plane enclosed within an encapsulating material** ..." in claim 1, as amended.

Therefore, Applicants believe the rejections under 35 U.S.C. 102(b) have been overcome.

Claim Rejections -- 35 U.S.C. 103 (a)

The Examiner rejected claim 9 under 35 U.S.C. 103(a) as being unpatentable over Garbelli et al. (U.S. Patent No. 5,825,628) in view of Hernandez et al. (U.S. Patent No. 4,734,818).

As discussed above, Garbelli et al. do not teach Applicants limitation of "... a ground plane connected to the ground lead, **the ground plane enclosed within an encapsulating material** ..." in claim 1, as amended. Claim 9 is dependant upon claim 1, as amended. Thus, the combination of Garbelli et al. with Hernandez et al. does not teach or suggest Applicants' claim 9.

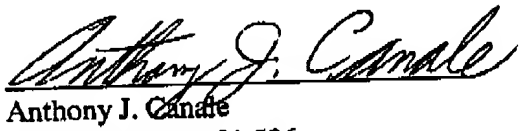
For the foregoing reasons, claim 9 is neither taught nor suggested, either individually or in combination, by Garbelli et al. or Hernandez et al. and is believed to be allowable over Garbelli et al. in view of Hernandez et al. Accordingly, Applicants respectfully request that the rejection of claim 9 over Garbelli et al. in view of Hernandez et al. be reconsidered and withdrawn.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

In light of the foregoing amendment and remarks, all of the claims now presented are believed to be in condition for allowance, and Applicants respectfully request that the outstanding rejections be withdrawn and this application be passed to issue at an early date.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully Submitted,
For: Fujio et al.

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Please amend claim 1 as follows:

1. (Twice Amended) A semiconductor integrated circuit device comprising:

a die connected to a ground lead and a power lead;

a ground plane connected to the ground lead, the ground plane enclosed within an encapsulating material;

an electrically insulating layer between said die and said ground plane; and

a decoupling capacitor having a first end and a second end, the first end connected to the ground lead and the second end connected to the power lead; ~~and~~

wherein the ~~an~~ encapsulating material ~~for encapsulating~~ encapsulates the die, the ground plane, the electrically insulating layer and the decoupling capacitor.